SONA COLLEGE OF TECHNOLOGY, SALEM-5

(An Autonomous Institution)

M.E-Electronics and Communication Engineering

(VLSI Design)

CURRICULUM and SYLLABI

[For students admitted in 2022-2023]

M.E / M.Tech Regulation 2019

Approved by BOS and Academic Council meetings

Sona College of Technology, Salem
(An Autonomous Institution)
Courses of Study for ME I Semester under Regulations 2019
Electronics and Communication Engineering
Branch: M.E. VLSI Design

S. No	Course Code	Course Title	Lecture	Tutorial	Practical	Credit	Total Contact Hours
Theory							
1.	P19VLD101	Graph Theory and Combinatorics	3	0	0	3	45
2.	P19VLD102	Advanced Digital System Design	3	1	0	4	60
3.	P19VLD103	CMOS Digital VLSI Design	3	0	0	3	45
4.	P19VLD104	Solid State Device Modeling and Simulation	3	0	0	3	45
5.	P19VLD105	DSP Integrated Circuits	3	0	0	3	45
6.	P19GE101	Research Methodology and IPR	2	0	0	2	30
7.	P19GE702	**Audit Course :** Stress Management by Yoga	2	0	0	0	30
Practical							
8.	P19VLD106	VLSI Design Laboratory	0	0	2	1	30
					Total Credits	**19**	

Approved by

Chairperson, Electronics and Communication Engineering BOS **Member Secretary, Academic Council** **Chairperson, Academic Council & Principal**
Dr.R.S.Sabeenian **Dr.R.Shivakumar** **Dr.S.R.R.Senthil Kumar**

Copy to:-
HOD/ECE, First Semester ME VLSI Students and Staff, COE

Sona College of Technology, Salem
(An Autonomous Institution)
Courses of Study for ME II Semester under Regulations 2019
Electronics and Communication Engineering
Branch: M.E. VLSI Design

S. No	Course Code	Course Title	Lecture	Tutorial	Practical	Credit	Total Contact Hours
Theory							
1	P19VLD201	Low Power VLSI Design	3	0	0	3	45
2	P19VLD202	VLSI for Signal Processing	3	0	0	3	45
3	P19VLD203	Design for Testability	3	0	0	3	45
4	P19VLD504	**Professional Elective –** Computer Aided Design of VLSI Circuits	3	0	0	3	45
5	P19VLD505	**Professional Elective –** Computer Architecture and Parallel Processing	3	0	0	3	45
6	P19VLD507	**Professional Elective –** Image Analysis and Computer Vision	3	0	0	3	45
7	P19GE701	**Audit Course –** English for Research Paper Writing	2	0	0	0	30
Practical							
8	P19VLD204	VLSI Design and Testing Laboratory	0	0	2	1	30
					Total Credits	**19**	

Approved by

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Dr.R.Shivakumar

Chairperson, Academic Council & Principal
Dr.S.R.R.Senthil Kumar

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ECE-VLSI
III

Sona College of Technology, Salem
(An Autonomous Institution)
Courses of Study for ME III Semester under Regulations 2019
Electronics and Communication Engineering
Branch: M.E. VLSI Design

S. No	Course Code	Course Title		Lecture	Tutorial	Practical	Credit	Total Hours
Theory								
1	**P19VLD506**	**Professional Elective-** Embedded Systems		3	0	0	3	45
2	**P19VLD511**	**Professional Elective-** Analysis and Design of Digital Integrated Circuits		3	0	0	3	45
3	**P19MIT601**	**Open Elective**	Python Programming	3	0	0	3	45
Practical								
4	**P19VLD301**	Project Phase - I		0	0	16	8	240
						Total Credits	**17**	**375**

Approved by

5/7/2023

Chairman, Electronics and Communication Engineering BOS
Dr.R.S.Sabeenian

Member Secretary, Academic Council
Dr.R.Shivakumar

Chairperson, Academic Council & Principal
Dr.S.R.R.Senthil Kumar

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M.E.VLSI
IV

Sona College of Technology, Salem
(An Autonomous Institution)
Courses of Study for ME IV Semester under Regulations 2019
Electronics and Communication Engineering
Branch: M.E. VLSI Design

S. No	Course Code	Course Title	Lecture	Tutorial	Practical	Credit	Total Contact Hours
Practical							
1	P19VLD401	Project Phase -II	0	0	28	14	420
					Total Credits	**14**	

Approved by

22/12/2023

Chairperson, Electronics and Communication Engineering BOS
Dr.R.S.Sabeenian

Member Secretary, Academic Council
Dr.R.Shivakumar 26/12/23

Chairperson, Academic Council & Principal
Dr.S.R.R.Senthil Kumar

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Sona College of Technology, Salem
(An Autonomous Institution)
Courses of Study for ME I Semester under Regulations 2019
Electronics and Communication Engineering
Branch: M.E. VLSI Design

S. No	Course Code	Course Title	Lecture	Tutorial	Practical	Credit	Total Contact Hours
Theory							
1.	P19VLD101	Graph Theory and Combinatorics	3	0	0	3	45
2.	P19VLD102	Advanced Digital System Design	3	1	0	4	60
3.	P19VLD103	CMOS Digital VLSI Design	3	0	0	3	45
4.	P19VLD104	Solid State Device Modeling and Simulation	3	0	0	3	45
5.	P19VLD105	DSP Integrated Circuits	3	0	0	3	45
6.	P19GE101	Research Methodology and IPR	2	0	0	2	30
7.	P19GE702	**Audit Course :** Stress Management by Yoga	2	0	0	0	30
Practical							
8.	P19VLD106	VLSI Design Laboratory	0	0	2	1	30
					Total Credits	**19**	

Approved by

Chairperson, Electronics and Communication Engineering BOS **Member Secretary, Academic Council** **Chairperson, Academic Council & Principal**
Dr.R.S.Sabeenian **Dr.R.Shivakumar** **Dr.S.R.R.Senthil Kumar**

Copy to:-
HOD/ECE, First Semester ME VLSI Students and Staff, COE

ELECTRONICS AND COMMUNICATION ENGINEERING

M. E. / VLSI DESIGN

SEMESTER – 1	GRAPH THEORY AND COMBINATORICS	L	T	P	C
P19VLD101		3	0	0	3

COURSE OUTCOMES

At the end of the course, the students will be able to

1. apply the counting principles to the real world problems.
2. solve the homogeneous and nonhomogeneous recurrence relations by the method of substitution and generating functions.
3. find the shortest path and minimal spanning tree of a weighted graph through algorithms.
4. find the matching and connectivity of a graph.
5. apply the concepts of planarity and coloring of a graph in a network problem.

CO / PO, PSO Mapping
(3/2/1 indicates strength of correlation) 3-Strong, 2-Medium, 1-Weak

COs	Programme Outcomes (POs) and Programme Specific Outcome (PSOs)													
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	2	2	2								3	
CO2	3	3	2	2	2								3	
CO3	3	3	2	2	2								3	
CO4	3	3	2	2	2								3	
CO5	3	3	2	2	2								3	

UNIT – I COMBINATORICS 9

Mathematical Induction – Basics of counting – Permutations and Combinations – Enumeration of permutations and combinations with constrained repetitions – Enumeration of permutations and combinations without constrained repetitions – Principle of inclusion and exclusion.

UNIT – II RECURRENCE RELATIONS 9

Generating functions of sequences – Calculating coefficients of generating functions – Recurrence relations – Solving recurrence relations by substitution and generating functions – Method of characteristic roots – Solutions of homogeneous and nonhomogeneous recurrence relations.

UNIT – III GRAPH THEORY 9

Fundamental concepts of graph – Paths – Cycles – Trails – Vertex degrees and counting – Trees and distance – Shortest path algorithm (Dijkstra's & Warshall's algorithm) – Spanning Trees – Optimization and trees (Prim's & Kruskal's algorithm).

UNIT – IV MATCHING AND CONNECTIVITY 9

Matching and coverings – Optimal assignment problem – Travelling salesman problem – Vertex and edge connectivity – Network flow problems.

UNIT – V COLORING AND PLANAR GRAPHS 9

Vertex coloring – Edge coloring – Chromatic polynomial – Color critical graphs – Planar graphs – Duality – Euler's formula – Characterization of planar graphs – Parameters of planarity.

Theory: 45 **Hours** Total: **45 Hours**

Note: Only statements of the theorems are considered in all the five units

TEXT BOOK:

1. D. B. West, "Introduction to Graph Theory", Pearson Publishers, 2nd Edition, 2017.

REFERENCE BOOKS:

1. N. Deo, "Graph Theory with Applications to Engineering and Computer Science", Dover Publishers, 1st Edition, 2016.
2. J. L. Mott, A. Kandel and T. P. Baker, "Discrete mathematics for Computer Scientists and Mathematics", Brady Publishers, 2nd Edition, 1985.
3. R. J. Wilson, "Introduction to Graph Theory", Pearson Publishers, 4th Edition, 2009.
4. R. Balakrishnan and K. Ranganathan, "A Textbook of Graph Theory", Springer Publishers, 2nd Edition, 2012.
5. V. K. Balakrishnan, "Graph Theory", Mc Graw Hill Publishers, 1st Edition, 2004.

Prof. S. JAYABHARATHI
Head / Department of Mathematics
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10. 05. 2019 **M.E / M.Tech Regulations 2019**

Course Outcomes

At the end of each unit, the students will be able to

1) Design and analyze the synchronous sequential circuits.
2) Design and analyze synchronous sequential circuits using ASM.
3) Design and analyze asynchronous sequential circuits.
4) Analyze and verify variable entered maps.
5) Design system controllers using combinational and sequential circuits.

CO / PO, PSO Mapping

(3/2/1 indicates strength of correlation) 3-Strong, 2-Medium, 1-Weak

COs	Programme Outcomes (POs) and Programme Specific Outcome (PSOs)													
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	P09	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	3	3	3	2	3	2	1	2	1	3	3	3
CO2	3	3	3	3	3	2	3	2	1	2	1	3	3	3
CO3	3	3	3	3	3	2	3	2	1	2	1	3	3	3
CO4	3	3	3	3	3	2	3	2	1	2	1	3	3	3
CO5	3	2	3	3	3	2	3	2	1	2	1	3	3	3

Unit I SYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 12

Structure and Operation of Clocked Synchronous Sequential Networks – Analysis of Clocked Synchronous Sequential Circuits – Modeling of Clocked Synchronous Sequential Network Behavior – Serial Binary Adder Using Mealy and Moore Networks – Sequence Recognizer – State Table Reduction – State Assignment – Design of Clocked Synchronous Sequential Circuits.

Unit II SYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN USING ASM 12

Algorithmic State Machine – ASM Charts – ASM Blocks – Sequence Recognition Using ASM Charts – State Assignments – ASM Transition Tables – ASM Excitation Tables – ASM Realization Using Discrete Gates – Multiplexers – Design of Iterative Circuits.

Unit III ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN **12**

Structure and Operation of Asynchronous Sequential Networks – Analysis of Asynchronous Sequential Circuit – Races and Hazards in Asynchronous Sequential Networks – Primitive Flow Table – Reduction of Input Restricted Flow Tables – Flow Table Reduction – State Assignment Problem and the Transition Table - Design of Asynchronous Sequential Circuits.

Unit IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES **12**

Programming logic device families – PLAs – PROMs - Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000.

Unit V SYSTEM DESIGN USING VERILOG **12**

Hardware Modelling with Verilog HDL – Logic System, Data Types and Operators For Modelling in Verilog HDL - Behavioural Descriptions in Verilog HDL – HDL Based Synthesis – Synthesis of Finite State Machines– structural modeling – compilation and simulation of Verilog code –Test bench - Realization of combinational and sequential circuits using Verilog – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor.

TOTAL : 60 HOURS

References

1) Donald G. Givone, "*Digital principles and Design"*, Tata McGraw Hill, 2013.

2) William I. Fletcher, "*An Engineering Approach to Digital Design"*, Prentice Hall India, 2009.

3) Charles H. Roth Jr,,"*Fundamentals of Logic design"*, Thomson Learning, 2004.

4) Nripendra N Biswas, "*Logic Design Theory"*, Prentice Hall of India, 2005.

P19VLD103 **CMOS DIGITAL VLSI DESIGN** **3 0 0 3**

Course Outcomes

At the end of each unit, the students will be able to -

1) Illustrate the VLSI design and fabrication processes of MOSFETs.
2) Describe and evaluate the MOSFET operations and modeling of MOSFETS.
3) Analyze and evaluate the static and switching characteristics of CMOS inverters..
4) Design combinational and sequential logic circuits using CMOS principles.
5) Analyze tradeoffs of the various circuit choices for each of the building block.

CO / PO, PSO Mapping

(3/2/1 indicates strength of correlation) 3-Strong, 2-Medium, 1-Weak

COs	Programme Outcomes (POs) and Programme Specific Outcome (PSOs)													
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	P09	PO10	PO11	PO12	PSO1	PSO2
CO1	2	2	1	2	2	3	3	2	1	2	2	1	3	3
CO2	1	2	2	2	1	2	3	2	1	2	2	1	3	2
CO3	2	2	3	3	1	2	2	2	2	1	1	1	3	3
CO4	2	2	2	3	3	2	3	2	2	2	2	1	3	3
CO5	1	2	2	3	3	3	2	2	2	1	1	2	2	2

Unit I INTRODUCTION AND FABRICATION OF MOSFETS **9**

Overview of VLSI Design Methodologies – VLSI Design Flow – Design Hierarchy – Concepts of Regularity, Modularity and Locality – VLSI Design Styles – Design Quality – Packaging Technology – Fabrication Process Flow Basic Steps – The CMOS n-Well Process – Layout Design Rules – Full-Custom Mask Layout Design.

Unit II MOS TRANSISTORS AND IT'S MODELING USING SPICE **9**

The MOS Structure – The MOS System under External Bias – Structure and Operation of MOS Transistor – MOSFET Current-Voltage Characteristics – MOSFET Scaling and Small-Geometry Effects – MOSFET Capacitances – Basic Concepts of Modeling of MOS – The LEVEL 1 Model Equations – The LEVEL 2 Model Equations – The LEVEL 3 Model Equations – State-of-the-Art MOSFET Models – Capacitance Models – Comparison of the SPICE MOSFET Models.

Unit III MOS INVERTERS AND CHARACTERISTICS 9

Static Characteristics of Resistive Load Inverter – Inverters with n-Type MOSFET Load – CMOS Inverter – Introduction of Switching Characteristics – Delay Time – Determination of delay Times – Inverter Design with Delay Constraints – Estimation of Interconnect Parasitics – Calculation of Interconnect Delay – Switching power Dissipation of CMOS inverters.

Unit IV COMBINATIONAL AND SEQUENTIAL CMOS LOGIC CIRCUITS 9

MOS Logic Circuits with Depletion nMOS Loads – CMOS Logic Circuits – CMOS Complex Logic Circuits – CMOS Transmission Gates – Behavior of Bistable Elements – CMOS SR Latch Circuit – CMOS Clocked Latch and CMOS Flip – Flop Circuits – CMOS D-Latch and CMOS Edge-Triggered Flip-Flop.

Unit V ARITHMETIC BUILDING BLOCKS AND MEMORY ARCHITECTURES 9

Data path circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs, Memory Architectures, and Memory control circuits.

TOTAL : 45 HOURS

References

1) Sung-Mo Kang and Yusuf Leblebici, "*CMOS Digital Integrated Circuits - Analysis and Design",* McGraw Hill Education (India) Pvt. Ltd., 3rd Edition, 2019
2) Bhaskar J., "*A Verilog HDL Primer",* B. S. Publications, 2nd Edition, 2018.
3) R. Jacob Baker, "*CMOS circuit design, Layout, and Simulation"*, John Wiley and Sons, 2012.
4) Neil H.E. Weste and Kamran Eshraghian, "*Principles of CMOS VLSI Design - A System Perspective",* Pearson Education ASIA, 2nd Edition, 2010
5) John P. Uyemura, "*Introduction to VLSI Circuits and Systems"*, John Wiley & Sons, Inc., 2006

P19VLD104 SOLID STATE DEVICE MODELING AND SIMULATION 3 0 0 3

Course Outcomes

At the end of each unit, the students will be able to –

1) Comprehend and analyze MOSFET device operation.
2) Analyze and illustrate the modeling technique for noise and its distortion
3) Design and analyze the modeling of BSIM4 MOSFET models
4) Design and evaluate other MOSFET models..
5) Analyze the modeling of passive devices and process variation

CO / PO, PSO Mapping

(3/2/1 indicates strength of correlation) 3-Strong, 2-Medium, 1-Weak

COs	Programme Outcomes (POs) and Programme Specific Outcome (PSOs)													
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	P09	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	3	3	2	2	3	1	1	2	2	3	3	2
CO2	3	3	3	3	3	2	3	2	2	2	2	3	3	2
CO3	3	3	3	3	3	2	3	1	1	2	2	3	3	2
CO4	3	3	3	3	3	2	3	1	2	2	2	3	3	2
CO5	3	3	3	3	3	2	3	2	1	2	2	3	3	2

Unit I MOSFET DEVICE PHYSICS AND OPERATION 9

The MOS Capacitor – Threshold Voltage – MOS Capacitance – MOS Charge Control Model – Basic MOSFET Operation – Basic MOSFET Modeling – Advanced MOSFET – Equivalent Circuit Representation of MOS Transistors.

Unit II NOISE MODELING AND DISTORTION ANALYSIS 9

Noise Sources in a MOSFET – Flicker Noise Modeling – The Physical Mechanisms of Flicker Noise – Flicker Noise Models – Thermal Noise Modeling – Existing Thermal Noise Models – HF Noise Parameters – Analytical Calculation of the Noise Parameters - Calculation of Distortion in Analog CMOS Circuits.

Unit III **BSIM4 MOSFET MODEL** **9**

An Introduction to BSIM4 – Gate Dielectric Model –Threshold Voltage Model – Channel Charge Model – Mobility Model – Source/Drain Resistance Model – I-V Model – Gate Tunneling Current Model – Substrate Current Models – Capacitance Models ..

Unit IV **OTHER MOSFET MODELS** **9**

Introduction - Model Features – Long-Channel Drain Current Model – Modeling Second-Order Effects of the Drain Current – SPICE Example – The Effect of Charge-Sharing – Modeling of Charge Storage Effects – Non-Quasi-Static Modeling – The Noise Model – MOS Model 9 – The MOSA1 Model.

Unit V **MODELING OF PASSIVE DEVICES AND PROCESS VARIATION** **9**

Introduction – Resistors – Well Resistor – Metal Resistor – Diffused Resistor – Poly Resistor – Capacitors – Poly-Poly Capacitors – Metal-Insulator-Metal Capacitors – MOSFET Capacitors – Junction Capacitors – Inductors – The Influence of Process Variation and Device Mismatch .

TOTAL : 45 HOURS

References

1) TrondYtterdal, Yuhua Cheng and Tor A. Fjeldly, "*Device Modeling for Analog and RF CMOS Circuit Design"*, John Wiley &1 edition, 2008.

2) Grasser, T., "*Advanced Device Modeling and Simulation"*, World Scientific Publishing Company, 2008..

3) Ben G. Streetman, "*Solid State Devices"*, Prentice Hall, 2015.

4) Carlos Galup-Montoro, Marco Cherem Schneider, "*MOSFET Modeling for Circuit Analysis and Design",* World Scientific Publishing Co. Pte. Ltd., 2007

P19VLD105 **DSP INTEGRATED CIRCUITS** **3 0 0 3**

Course Outcomes

At the end of each unit, the students will be able to –

1) Design and apply standard DSP and other DSP systems used in ICs.
2) Design and illustrate the concepts of DSP systems, DFT, FFT and DCT.
3) Design the digital filters IIR and FIR for signal processing applications
4) Examine and synthesize the DSP architectures and implement it on PEs and bit serial PEs.
5) Design and evaluate recent trends in DSP processors.

CO / PO, PSO Mapping

(3/2/1 indicates strength of correlation) 3-Strong, 2-Medium, 1-Weak

COs	Programme Outcomes (POs) and Programme Specific Outcome (PSOs)													
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	P09	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	3	3	3	2	1	1	1		2	3	3	3
CO2	3	3	3	3	3	2	1	1	1		2	3	3	3
CO3	3	3	3	3	3	2	1	1	1		2	3	3	3
CO4	3	3	3	3	3	2	1	1	1		2	3	3	3
CO5	3	3	3	3	3	2	1	1	1		2	3	3	3

Unit I DSP INTEGRATED CIRCUITS **09**

Standard Digital Signal Processors – Application Specific IC's for DSP – DSP System–DSP System Design – Partitioning Techniques – Integrated Circuit Design – MOS transistors – MOS logic – VLSI process Technologies – Trends in CMOS Technologies.

Unit II DIGITAL SIGNAL PROCESSING **09**

Digital Signal Processing – Sampling of Analog Signals – Selection of Sample Frequency – Signal-Processing Systems – Frequency Response – Transfer Functions – Signal Flow Graphs – Filter Structures – Adaptive DSP Algorithms – DFT – The Discrete Fourier Transform – FFT – The Fast Fourier Transform Algorithm – Discrete Cosine Transforms.

Unit III DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS **09**

FIR Filters – FIR Filter Structures - FIR chips – IIR filters – Specifications of IIR Filters – Mapping of Analog Transfer Functions – Mapping of Analog Filter Structures – Finite Word Length Effects –Parasitic Oscillations – Scaling of Signal Levels – Round-Off Noise – Measuring Round-Off Noise – Coefficient Sensitivity – Sensitivity and Noise

Unit IV DSP ARCHITECTURES AND SYNTHESIS OF DSP ARCHITECTURES **09**

Introduction – DSP System Architectures – Standard DSP Architecture – Ideal DSP Architectures – Multiprocessors and Multi-Computers – Systolic and Wave Front Arrays – Shared Memory Architectures – Mapping of DSP Algorithms onto Hardware – Implementation Based on Complex PEs – Shared Memory Architecture With Bit – Serial PEs.

Unit V DSP PROCESSOR **09**

Introduction of TMS320C6748 Processor – Features – CPU Architecture of C6748– Memory Architecture – Addressing Modes – Assembly Language Instructions – Pipeline Operation – Interrupts – Peripherals.

TOTAL : 45 HOURS

References

1) Lars Wanhammer, "*DSP Integrated Circuits"*, Academic press, New York, Reprint 2014

2) Venkataramani B. and Bhaskar M., "*Digital Signal Processors – Architecture, Programming and Applications"*, Tata McGraw – Hill Publishing Company Limited, New Delhi, 2017..

3) Emmanuel C. I. Feachor, Barrie W. Jervis, "*Digital signal processing – A Practical Approach"*, 2nd Edition, Pearson Education, Asia 2007..

4) Bayoumi&Magdy A., "*VLSI Design Methodologies for Digital Signal Processing Architectures"*, BS Publications, 2012.

P19VLD106 **VLSI DESIGN LABORATORY** **0 0 2 1**

Course Outcomes

At the end of the experiments, the students will be able to -

1) Design and analysis the digital systems using Verilog HDL
2) Implement the digital system design in FPGA Board and analyze the same for performance
3) Design the NMOS, CMOS Logic circuits and analyze the characteristics of the same

CO / PO, PSO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2-Medium, 1-Weak														
COs	Programme Outcomes (POs) and Programme Specific Outcome (PSOs)													
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	P09	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	3	3	3	3	3	2	1	1	1	3	3	3
CO2	3	2	1	3	3	1	3	2	1	1	1	3	3	3
CO3	3	3	3	3	3	3	3	2	1	1	1	3	3	3

List of Experiments

1) Design of NMOS and CMOS Inverters - DC and transient characteristics and switching times
2) Design of CMOS logic gate circuits
   i) Static Logic
   ii) Dynamic Logic
   iii) Domino Logic
3) Design of combinational circuits using Verilog and implement in FPGA.
   i) Multiplexer and De-Multiplexer
   ii) Encoder and Decoder
   iii) Comparator
4) Design of sequential circuits using Verilog and implement in FPGA
   i) Shift Registers
   ii) Counters
5) Design and implementation of ALU using FPGA and Verilog HDL
6) Design of FIR filters CORDIC using FPGA and Verilog HDL
7) Design and implementation of floating point multiplier
8) Design and implementation of Stepper Motor using FPGA
9) Design and implementation of traffic controller using FPGA

TOTAL: 30 HOURS

P19GE101 RESEARCH METHODOLOGY AND IPR 2 0 0 2

COURSE OUTCOMES

At the end of the course, the student will be able to

1. Review the literature of the research problem
2. Choose appropriate data collection and sampling method according to the research problem.
3. Interpret the results of research and communicate effectively with their peers
4. Explain the Importance of intellectual property rights
5. Evaluate trade mark, develop and register patents

CO/PO, PSO Mapping
(3/2/1 indicates strength of correlation) 3-Strong, 2-Medium, 1-Weak

COs	Programme Outcomes (POs) and Programme Specific Outcome (PSOs)												
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	P09	PO10	PO12	PSO1	PSO2
CO1	3	3	3	3	2						3	3	3
CO2	3	3	3	3	2						3	3	3
CO3	3	3	3	3	2						3	3	3
CO4	3	3	3	3	2						3	3	3
CO5	3	3	3	3	2			3			3	3	3

UNIT I INTRODUCTION TO RESEARCH METHODS 6

Definition and Objective of Research, Various steps in Scientific Research, Types of Research, Criteria for Good Research, Defining Research Problem, Research Design , Case Study Collection of Primary and Secondary Data, Collection Methods: Observation, Interview, Questionnaires, Schedules,

UNIT II SAMPLING DESIGN AND HYPOTHESIS TESTING 6

steps in Sampling Design, Types of Sample Designs, Measurements and Scaling Techniques - Testing of hypotheses concerning means (one mean and difference between two means - one tailed and two tailed tests), concerning variance – one tailed Chi-square test.

UNIT III INTERPRETATION AND REPORT WRITING 6

Techniques of Interpretation, Precaution in Interpretation, Layout of Research Report, Types of Reports, Oral Presentation, Mechanics of Writing Research Report

UNIT IV INTRODUCTION TO INTELLECTUAL PROPERTY 6

Introduction, types of intellectual property, international organizations, agencies and treaties, importance of intellectual property rights, Innovations and Inventions trade related intellectual property rights.

16-09-2022

Dr. J. AKILANDESWARI
PROFESSOR & HEAD
Department of Information Technology
SONA COLLEGE OF TECHNOLOGY
SALEM-636 005

UNIT V TRADE MARKS, COPY RIGHTS AND PATENTS 6

Purpose and function of trade marks, acquisition of trade mark rights, trade mark registration processes, trademark claims –trademark Litigations- International trademark law

Fundamental of copy right law, originality of material, rights of reproduction, rights to perform the work publicly, copy right ownership issues, copy right registration, notice of copy right, international copy right law.

Law of patents: Foundation of patent law, patent searching process, ownership rights and transfer

THEORY: 30 Hours TUTORIAL: - PRACTICAL: - TOTAL: 30 Hours

TEXT BOOKS

1. C.R. Kothari, Gaurav Garg, Research Methodology Methods and Techniques ,4th Edition, New Age International Publishers, 2019.
2. Deborah E. Bouchoux, "Intellectual Property: The Law of Trademarks, Copyrights, Patents, and Trade Secrets", Delmar Cengage Learning, 4th Edition, 2012.
3. Prabuddha Ganguli, "Intellectual Property Rights: Unleashing the Knowledge Economy", Tata Mc Graw Hill Education, 1st Edition, 2008.

REFERENCE BOOKS

1. Panneerselvam, R., Research Methodology, Second Edition, Prentice-Hall of India, New Delhi, 2013.
2. Ranjith Kumar, Research Methodology – A step by step Guide for Begineers, 4th edition, Sage publisher, 2014.
3. D Llewelyn & T Aplin W Cornish, "Intellectual Property: Patents, Copyright, Trade Marks and Allied Rights", Sweet and Maxwell, 1st Edition, 2016.
4. Ananth Padmanabhan, "Intellectual Property Rights-Infringement and Remedies", Lexis Nexis, 1st Edition, 2012.
5. Ramakrishna B and Anil Kumar H.S, "Fundamentals of Intellectual Property Rights: For Students, Industrialist and Patent Lawyers", Notion Press, 1st Edition, 2017.
6. M.Ashok Kumar and Mohd.Iqbal Ali :"Intellectual Property Rights" Serials Pub

16-09-2022

Dr. J. AKILANDESWARI
PROFESSOR & HEAD
Department of Information Technology
SONA COLLEGE OF TECHNOLOGY
SALEM-636 005

P19GE702 **Stress Management by Yoga**

2000

Course Outcomes:

At the end of completion of this course, students will be able to

1. Develop physical and mental health thus improving social health
2. Increase immunity power of the body and prevent diseases
3. Accelerate memory power
4. Achieve the set goal with confidence and determination
5. Improve stability of mind, pleasing personality and work with awakened wisdom

UNIT – I **6**

Yoga-Introduction - Astanga Yoga- 8 parts-Yam and Niyam etc.- Do`s and Don'ts in life- Benefits of Yoga and Asana- Yoga Exercise- and benefits- Pranayam Yoga- Nadi suthi, Practice and Spinal Sclearance Practice- Regularization of breathing techniques and its effects-Practice and kapalapathy practice.

UNIT – II **6**

Neuromuscular breathing exercise and Practice- Magarasa Yoga, 14 points Acupressure techniques and practice- Body relaxation practice and its benefits- Raja Yoga- 1.Agna – explanation and practice- Activation of Pituitary- Raja Yoga- 2. Santhi Yoga-Practice- Balancing of physical and mental power.

UNIT – III **6**

Raja Yoga- 3. Sagasrathara yoga –practice- Activation of dormant brain cells-Kayakalpa-theory- Kayakalpa –practice-Yogic exercise to improve physical and mental health and practice-Asanas –explanation-Practice-benefits

UNIT –IV **6**

Sun namaskar- 12 poses-explanation and practice-Yoga –Asana-Padmasana, vajrasana,chakrasana, viruchasana etc-Stress management with Yoga-Role of women and Yoga

Equality, nonviolence, Humanity, Self- control- Food and yoga Aware of self-destructive habits

Avoid fault thinking (thought analysis-Practice)-Yoga Free from ANGER (Neutralization of anger)& practice

UNIT – V **6**

Moralisation of Desire & practice- Punctuality-Love-Kindness-Compassion Eradication of worries-Practice -Personality development, positive thinking-Good characters to lead a moral life

How to clear the polluted mind- Benefits of blessing- Five- fold culture –explanation- Karma Yoga Practice In Geetha- Sense of duty-Devotion, self- reliance, confidence, concentration, truthfulness, cleanliness.

Reference Books

1. 'Yogic Asanas for Group Tarining-Part-I" Janardan Swami Yogabhyasi Mandal, Nagpur
2. "Rajayoga or conquering the Internal Nature" by Swami Vivekananda, AdvaitaAshrama (Publication Department), Kolkata

Total: 30 hours

Dr. M. Renuga
BoS – Chairperson,
Science & Humanities
HOD / H&L

Sona College of Technology, Salem
(An Autonomous Institution)
Courses of Study for ME II Semester under Regulations 2019
Electronics and Communication Engineering
Branch: M.E. VLSI Design

S. No	Course Code	Course Title	Lecture	Tutorial	Practical	Credit	Total Contact Hours
Theory							
1	P19VLD201	Low Power VLSI Design	3	0	0	3	45
2	P19VLD202	VLSI for Signal Processing	3	0	0	3	45
3	P19VLD203	Design for Testability	3	0	0	3	45
4	P19VLD504	**Professional Elective –** Computer Aided Design of VLSI Circuits	3	0	0	3	45
5	P19VLD505	**Professional Elective –** Computer Architecture and Parallel Processing	3	0	0	3	45
6	P19VLD507	**Professional Elective –** Image Analysis and Computer Vision	3	0	0	3	45
7	P19GE701	**Audit Course –** English for Research Paper Writing	2	0	0	0	30
Practical							
8	P19VLD204	VLSI Design and Testing Laboratory	0	0	2	1	30
					Total Credits	**19**	

Approved by

Chairperson, Electronics and Communication Engineering BOS
Dr.R.S.Sabeenian

Member Secretary, Academic Council
Dr.R.Shivakumar

Chairperson, Academic Council & Principal
Dr.S.R.R.Senthil Kumar

Copy to:-
HOD/ECE, Second Semester ME VLSI Students and Staff, COE

P19VLD201 **LOW POWER VLSI DESIGN** **3 0 0 3**

Course Outcomes

At the end of each unit, the students will be able to

1) Evaluate about the sources of power consumption in CMOS and hierarchy of limits
2) Calculate the power estimation in CMOS at logic level and circuit level.
3) Analyze the synthesis and software design for low power
4) Analyze the SOI CMOS Devices
5) Design SOI CMOS digital and analog circuits

CO / PO, PSO Mapping
(3/2/1 indicates strength of correlation) 3-Strong, 2-Medium, 1-Weak

COs	Programme Outcomes (POs) and Programme Specific Outcome (PSOs)													
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	P09	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	3	2	1								3	2
CO2	3	3	2	2	1		2						3	2
CO3	3	3	2	3	2	1	2	1					3	2
CO4	3	3	3	3	2			1			2		3	2
CO5	3	3	2	2	2		2				2		3	2

Unit I **POWER DISSIPATION IN CMOS** **9**

Introduction – Sources of Power Dissipation – Designing for Low power – Physics of Power Dissipation in MOSFET Devices – Power Dissipation in CMOS – Hierarchy of Limits of Power – Fundamental-Material- Device-Circuit and System limits

Unit II **POWER ESTIMATION** **9**

Modeling of Signals – Signal Probability Calculation – Probabilistic Techniques for Signal Activity Estimation – Statistical Techniques – Estimation of Glitching Power – Sensitivity Analysis – Power Estimation Using Input Vector Compaction – Power Dissipation in Domino CMOS – Circuit Reliability – Power Estimation at the Circuit Level – High Level Power Estimation – Information-Theory-Based Approaches – Estimation of Maximum power.

Unit III **SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER** **9**

Behavioral Level Transforms – Logic Level Optimization for Low power – Circuit Level – Sources of Software Power Dissipation – Software Power Estimation – Software Power Optimizations – Automated Low-Power Code Generation – Co-design for Low Power.

Unit IV SOI CMOS DEVICE **9**

Introduction – Basic SOI Technology – Back Gate Bias Effects – Short Channel Effects – Narrow Channel Effects – Mobility – Floating Body Effects – Subthreshold Behavior – Impact Ionization – Breakdown – Transient-Induced Leakage – Self-Heating – Hot Carriers – Accumulation-Mode Devices.

Unit V SOI CMOS DIGITAL AND ANALOG CIRCUITS **9**

Static and Dynamic Logic Circuits – DRAM – SRAM – CAM – Gate Array – CPU – Multiplier and DSP – Frequency Divider – SOI Op Amps – Filters – ADC and DAC – Sigma – Delta ADC – RF Circuits Sigma – Low Noise Amplifier – Mixer – Voltage Controlled Oscillator.

TOTAL : 45 HOURS

References

1) Roy K. and Prasad S.C. , "*Low Power CMOS VLSI circuit design,"* Wiley,2011.

2) James B. Kuo, Shin chia Lin, *"Low voltage SOI CMOS VLSI Devices and Circuits"*, John Wiley and sons, inc 2008.

3) DimitriosSoudris, ChirstianPignet, Costas Goutis, "*Designing CMOS Circuits For Low Power"*, Kluwer,2010.

4) Kuo J.B and Lou J.H, "*Low voltage CMOS VLSI Circuits"*, Wiley 2017

5) Roy K. and Prasad S.C. , "*Low Power CMOS VLSI circuit design,"* Wiley,2011.

P19VLD202 **VLSI FOR SIGNAL PROCESSING** **3 0 0 3**

Course Outcomes

At the end of each unit, the students will be able to

1) Develop different algorithm for DSP systems and discuss about the pipelining and parallel processing.
2) Analyze the different techniques of retiming, folding and unfolding.
3) Design IIR filters for fast convolution, pipelining and parallel processing
4) Design the different types of multipliers and CSD Representation of VLSI systems
5) Apply synchronous and asynchronous pipelining in DSP Processors

CO / PO, PSO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2-Medium, 1-Weak														
COs	Programme Outcomes (POs) and Programme Specific Outcome (PSOs)													
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	P09	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3		3	3	3		3					3	3
CO2	3	3		3	3	3		3					3	3
CO3	3	3		3	3	3		3					3	3
CO4	3	3		3	3	3		3					3	3
CO5	3	3		3	3	3		3					3	3

Unit I INTRODUCTION TO DSP SYSTEMS **9**

Introduction to DSP Systems –Typical DSP Algorithms – Iteration Bound – Data Flow Graph Representations – Loop Bound and Iteration Bound – Algorithms for Computing Iteration Bound – Pipelining and Parallel Processing –Pipelining of FIR Digital Filters – Parallel Processing – Pipelining and Parallel Processing for Low Power..

Unit II RETIMING, FOLDING AND UNFOLDING **9**

Retiming – Definitions and Properties – Retiming Techniques – Unfolding – an Algorithm for Unfolding – Properties of Unfolding –Applications – Sampling Period Reduction – Parallel Processing –Folding – Folding Transformation – Register Minimizing Techniques – Register Minimization in Folded Architectures.

Unit III FAST CONVOLUTION **9**

Fast Convolution – Cook-Toom Algorithm –modified Cook-Toom algorithm– Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with powerof-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

Unit IV BIT-LEVEL ARITHMETIC ARCHITECTURES 9

Bit-Level Arithmetic Architectures – Parallel Multipliers – Baugh-Wooley Multipliers – Interleaved Floor – Plan and Bit-Plane – Based Digital Filters – Design of Lyon's Bit-Serial Multipliers using Horner's Rule – Bit-Serial FIR Filter –CSD Representation – CSD Multiplication using Horner's Rule for Precision Improvement – Distributed Arithmetic

Unit V PROGRAMMING DIGITAL SIGNAL PROCESSORS 9

Synchronous – Wave and Asynchronous Pipelining – Synchronous Pipelining and Clocking Styles – Clock Skew and Clock Distribution in Bit-Level Pipelined VLSI Designs –Wave Pipelining – Asynchronous Pipelining – Programming Digital Signal Processors – General Architecture with Important Features.

TOTAL : 45 HOURS

References

1) Keshab K. Parhi, " *VLSI Digital Signal Processing Systems*", Design and implementation , Wiley, Interscience, 2007.

2) U. Meyer – Baese, " *Digital Signal Processing with Field Programmable Gate Arrays*", Springer, Indian Reprint, 2014.

P19VLD203 **DESIGN FOR TESTABILITY** **3 0 0 3**

Course Outcomes

At the end of each unit, the students will be able to -

1) Analyze the modeling of faults and types of simulation for testing circuits and systems
2) Design and analyze test generation of combinational circuits and testable designs
3) Design and analyze test generation of sequential circuits and testable designs.
4) Design and evaluate the test pattern generation of Built In Self Test.
5) Synthesize and analyze different fault diagnosis in combinational and sequential circuits.

CO / PO, PSO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2-Medium, 1-Weak														
COs	Programme Outcomes (POs) and Programme Specific Outcome (PSOs)													
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	P09	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	3	3	2	2	3	1		2	2	3	3	2
CO2	3	3	3	3	3	2	3	2		2	2	3	3	2
CO3	3	3	3	3	3	2	3	1		2	2	3	3	2
CO4	3	3	3	3	3	2	3	1		2	2	3	3	2
CO5	3	3	3	3	3	2	3	2		2	2	3	3	2

Unit I TESTING AND FAULT MODELLING **9**

Introduction to Testing – Faults in Digital Circuits – Modeling of Faults – Logical Fault Models – Fault Detection and Redundancy – Fault Equivalence and Fault Location – Fault Dominance – Logic Simulation – Types of Simulation – Compiled Simulation – Event Driven Simulation – Delay Models – Gate Level Event-Driven Simulation

Unit II TEST GENERATION OF COMBINATIONAL CIRCUITS **9**

Test Generation of Combinational Logic Circuits – One Dimensional Path Sensitization – Boolean Difference – D-Algorithm – Path Oriented Decision Making – Detection of Multiple Faults in Combinational Logic Circuits – Testable Combinational Logic Circuit Design –The Reed-Muller Expansion Techniques – Three Level OR- AND - OR Design – Use of Control Logic – Syndrome Testable Design.

Unit III TEST GENERATION OF SEQUENTIAL CIRCUITS **9**

Test Generation of Sequential Circuits – Testing of Sequential Circuits as Iterative Combinational Circuits – State Table Verification – Random Testing – Transition Count Testing – Signature Analysis – Design of Testable Sequential Circuits – Scan Path Technique – Level Sensitive Scan Design – Random Access Scan Technique

Unit IV BUILT IN SELF – TEST **9**

Introduction – Test Pattern Generation for BIST – Exhaustive Testing – Pseudorandom Testing – Pseudo-Exhaustive Testing – Specific BIST Architectures – Built In Evaluation and Self Test – Random Test Socket – LSSD on Chip Self Test – Self-Testing Using MISR and Parallel SRSG – Concurrent BIST Architecture – Random Test Data – Circular Self Test Path – Built In Logic Block Observation.

Unit V FAULT DIAGNOSIS **9**

Logic Level Diagnosis – Fault Dictionary- Guided Probe Testing – Diagnosis by UUT Reduction – Fault Diagnosis for Combinational Circuits – Expert Systems for Diagnosis – Effect Cause Analysis – Self Checking Design – Application of Error Detecting and Error Correcting Codes – Multiple Bit Errors – Checking Circuits and Self Checking – Self Checking Checkers – Parity Check Function – Totally Self Checking Checkers.

TOTAL : 45 HOURS

References

1) Parag K. Lala, "*Fault Tolerant and Fault Testable Hardware Design*", BS Publications, 2009.

2) Abramovici M, Breuer M.A. and Friedman A.D., "*Digital Systems and Testable Design*", Jaico Publishing House, 2004

3) Bushnell M.L and Agrawal V. D., "*Essentials of Electronic Testing for Digital*", Memory and Mixed-Signal VLSI Circuit", Kluwar Academic Publishers, 2009

4) Crouch A.L,"*Design for Test for Digital IC's and Embedded Core System*", Prentice Hall International, 2002.

P19VLD504 COMPUTER AIDED DESIGN OF VLSI CIRCUITS 3 0 0 3

Course Outcomes

At the end of the course, the student will be able to

1) Analyze the VLSI design methodologies and algorithmic graph theory.
2) Analyze and illustrate layout design rules, placement and partitioning.
3) Design and analyze floor planning and routing concept.
4) Examine and verify the various modeling of simulation.
5) Analyze and illustrate synthesis and scheduling.

CO / PO, PSO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2-Medium, 1-Weak														
COs	Programme Outcomes (POs) and Programme Specific Outcome (PSOs)													
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	P09	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	3	3	2	2	3	1		2	2	3	3	3
CO2	3	3	3	3	3	2	3	1		2	2	3	3	3
CO3	3	3	3	3	3	2	3	1		2	2	3	3	3
CO4	3	3	3	3	3	2	3	1		2	2	3	3	3
CO5	3	3	3	3	3	2	3	1		2	2	3	3	3

Unit I VLSI DESIGN METHODOLOGIES AND ALGORITHMIC GRAPHY THEORY 9

Introduction to VLSI Design Methodologies – VLSI Design Automation Tools – Algorithmic Graph Theory and Computational Complexity – Tractable and Intractable Problems – General Purpose Methods for Combinatorial Optimization

Unit II PLACEMENT AND PARTITIONING 9

Layout Compaction – Design Rules - Problem Formulation – Algorithms for Constraint Graph Compaction –Placement And Partitioning – Circuit Representation – Wire length Estimation– Placement Algorithms – Partitioning.

Unit III FLOORPLANNING AND ROUTING **9**

Floor planning Concepts – Shape Functions and Floor Plan Sizing – Types of Local Routing Problems – Area Routing – Channel Routing – Global Routing – Algorithms for Global Routing.

Unit IV SIMULATION AND VERIFICATION **9**

VLSI Simulation – Gate-Level Modeling And Simulation – Switch-Level Modeling and Simulation – Combinational Logic Synthesis – Binary Decision Diagrams – Two Level Logic Synthesis.

Unit V HIGH LEVEL SYNTHESIS **9**

Hardware Models for High Level Synthesis – Internal Representation of the Input Algorithm– Allocation-Assignment and Scheduling – Scheduling Algorithm – Assignment problem – High Level Transformations.

TOTAL : 45 HOURS

References

1) Gerez S.H., "*Algorithms for VLSI Design Automation"*, John Wiley & Sons,2009.

2) Sherwani N.A., "*Algorithms for VLSI Physical Design Automation*"Kluwar Academic Publishers, 2013

3) Drechsler, R., "*Evolutionary Algorithms for VLSI CAD"*, Kluwer Academic Publishers, Boston, 2010.

4) Hill, D., Shugard D., Fishburn J. and Keutzer K., "*Algorithms and Techniques for VLSI Layout Synthesis"*, Kluwer Academic Publishers, Boston, 2011.

P19VLD505 COMPUTER ARCHITECTURE AND PARALLEL PROCESSING 3 0 0 3

Course Outcomes

At the end of the course, the student will be able to

1) Analyze the advanced concepts of parallel processing
2) Apply the memory hierarchy for multiprocessor system
3) Analyze the design structures of pipelined and multiprocessor systems
4) Analyze the system architecture with parallel, vector and scalable architecture for building high-performance computers
5) Apply the concept in parallel processing concept in various architecture

CO / PO, PSO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2-Medium, 1-Weak														
COs	Programme Outcomes (POs) and Programme Specific Outcome (PSOs)													
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	P09	PO10	PO11	PO12	PSO1	PSO2
CO1	2	3	2	3	2	2	3	2	1	2	2	3	3	3
CO2	3	2	3	1	3	3	3	2	2	2	2	3	3	3
CO3	2	3	3	3	1	2	3	2	1	2	2	1	3	3
CO4	2	2	3	3	3	2	3	2	2	2	3	3	3	3
CO5	2	2	3	3	3	2	3	2	1	2	3	3	3	3

Unit I PRINCIPLES OF PARALLEL PROCESSING 6

Multiprocessors and Multicomputers – Multivector and SIMD Computers – PRAM and VLSI Models – Conditions of Parallelism – Program Partitioning and Scheduling- Program Flow Mechanisms – Parallel Processing Applications – Speed Up Performance Law.

Unit II PROCESSOR AND MEMORY ORGANIZATION 6

Advanced Processor Technology – Superscalar and Vector Processors – Memory Hierarchy Technology – Virtual Memory Technology – Cache Memory Organization – Shared Memory Organization.

Unit III PIPELINE AND PARALLEL ARCHITECTURE **6**

Linear Pipeline Processors – Non Linear Pipeline Processors – Instruction Pipeline Design –Arithmetic Design – Superscalar and Super Pipeline Design – Multiprocessor System Interconnects – Message Passing Mechanisms.

Unit IV VECTOR, MULTITHREAD AND DATAFLOW ARCHITECTURE **6**

Vector Processing Principle – Multi-Vector Multiprocessors – Compound Vector Processing- Principles of Multithreading – Fine Grain Multi-Computers – Scalable and Multithread Architectures – Dataflow and Hybrid Architectures

Unit V SOFTWARE AND PARALLEL PROCESSING **6**

Parallel Programming Models – Parallel Languages and Compilers – Parallel Programming Environments Synchronization and Multiprocessing Modes – Message Passing Program Development – Mapping Programs onto Multi Computers – Multiprocessor UNIX Design Goals – MACH/OS Kernel Architecture – OSF/1 Architecture and Applications.

TOTAL : 45 HOURS

References

1) Kai Hwang, "*Advanced Computer Architecture*", TMH 2017, 3rd edition.

2) DezsoSima,TerenceFountain,PeterKacsuk,"*AdvancedComputerarchitecture–A designSpaceApproach*" ,PearsonEducation,2003.

3) John P.Shen, "*Modern processor design. Fundamentals of super scalar processors*", Tata McGraw Hill 2013.

4) Harry F. Jordan Gita Alaghband, " *Fundamentals of parallel Processing*", Pearson Education , 2003

5) Richard Y.Kain, " *Advanced computer architecture –A systems Design Approach*", PHI, 2003

6) Quinn M.J, "*Designing efficient Algorithms for parallel computer*", McGraw Hill International, 1994.

7) William Stallings, "*Computer Organization and Architecture*", McMillan Publishing Company, 2013.

P19VLD507 IMAGE ANALYSIS AND COMPUTER VISION 3 0 0 3

Course Outcomes

At the end of each unit, the students will be able to –

1) Implement image enhancement algorithms.
2) Apply image transforms for different image applications
3) Perform different segmentation and restoration
4) Implement different compression techniques
5) Develop algorithms for computer vision problems

CO / PO, PSO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2-Medium, 1-Weak														
COs	Programme Outcomes (POs) and Programme Specific Outcome (PSOs)													
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	P09	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	2	3	3	1	1			1	2	1	3	3
CO2	3	3	2	3	3	1	1			1	2	1	3	3
CO3	3	3	2	3	3	1	1			1	2	1	3	3
CO4	3	3	2	3	3	1	1			1	2	1	3	3
CO5	3	3	2	3	3	1	1			1	2	1	3	3

Unit I IMAGE ENHANCEMENT 9

Digital Image fundamentals - Image sampling - Quantization - Spatial domain filtering - Image negative - Contrast stretching, Gray level slicing - Histogram equalization - Smoothing filters, Sharpening filters, Maximum filter, Minimum filter, Median filter.

Unit II IMAGE TRANSFORMS 9

2D transforms - DFT - DCT - Walsh - Hadamard - Slant - Haar - KLT - SVD - Wavelet transform.

Unit III IMAGE RESTORATION AND SEGMENTATION 9

Image restoration - degradation model - Unconstrained and Constrained restoration - Inverse filtering - Wiener filtering - Image segmentation - Thresholding - Edge detection - Region based segmentation.

Unit IV IMAGE COMPRESSION **6**

Need for data compression - Huffman - Arithmetic coding - LZW technique - Vector Quantization - JPEG – MPEG

Unit V COMPUTER VISION **12**

Texture classification - Feature extension - Markov Random Field Matrix – Gray Level Co –occurrence Matrix – Gray Level Weight Matrix , Multi Resolution Combined Statistical and Spatial Frequency method, character recognition- zoning approaches, Medical Image Analysis – Diabetic Retinopathy – Glaucoma.

TOTAL : 45 HOURS

References

1) Rafael C.Gonzalex, Richard E.Woods, "*Digital Image Processing, Pearson Education. Inc"*., Forth Edition, 2018

2) Anil K.Jain, "*Fundamentals of Digital Image Processing*", Prentice Hall of India, 2004

3) Milan Sonka, Vaclav Hlavac and Roger Boyle, "*Image Procesing, Analysis and Machine Vision*", Brookes/Cole, Vikas Publishing House, 2nd edition, 1999

4) Jayaraman S Esakkirajan and Veerakumar, "Digital Image Processing", McGraw Hill Education; July 2017

5) Sid Ahmed, M.A., "*Image Processing Theory, Algorithms and Architectures*", Mc Graw Hill, 1995

6) Richard Szeliski, "*Computer Vision Algorithms and Applications*", Springer Verlag London Limited, 2011

7) Sabeenian R.S., "*Digital Image Processing*", Sonaversity publication, Second Edition, 2010

8) Annadurai S., R. Shanmugalakshmi, "*Fundamentals of Digital Image Processing*", Pearson Education India, 2007

9) Sridhar.S, "*Digital Image Processing*", Oxford University Press, First Edition, 2011

10) Kenneth R. Castleman, "*Digital Image Processing*", Pearson, 2009

P19VLD204 VLSI DESIGN AND TESTING LABORATORY 0 0 2 1

Course Outcomes

At the end of the course, the student will be able to

1) Design and simulate the performance analysis of source followers, and OP- AMPs, different types of current mirrors.
2) Design and simulate test and verification using system Verilog
3) Implementation of the real time application using Embedded Microcontroller

CO / PO, PSO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2-Medium, 1-Weak														
COs	Programme Outcomes (POs) and Programme Specific Outcome (PSOs)													
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	P09	PO10	PO11	PO12	PSO1	PSO2
CO1	2	2	2	3	3	2	2	3	1	1	2	3	2	3
CO2	2	2	2	3	3	2	2	3	1	1	2	3	2	3
CO3	2	2	2	3	3	2	2	3	1	1	2	3	2	3

List of Experiments

1) Design and simulate frequency response and noise analysis of any Source followers
2) Design and simulate operational amplifier performance parameters - One-stage Op Amps, Two-stage Op Amps
3) Design and simulate cascode current mirrors and active current mirrors
4) Design and implementation of BIT - SLICE using FPGA
5) Design and Simulation of Gate-level modeling
6) Design and Simulation of Switch-level modeling
7) Verification of combinational circuits using system Verilog
8) Verification of sequential circuits using system Verilog
9) Implementation of Elevator controller using Embedded Microcontroller
10) Implementation of model train controller using Embedded Microcontroller

TOTAL: 30 HOURS

AUDIT COURSE

P19GE701 **English for Research Paper Writing**

2 0 0 0

Course Outcomes:

At the end of the course, the students will be able to

- Demonstrate research writing skills both for research articles and thesis
- Frame suitable title and captions as sub-headings for articles and thesis
- Write each section in a research paper and thesis coherently
- Use language appropriately and proficiently for effective written communication
- Exhibit professional proof-reading skills to make the writing error free

Unit – I **6**

Planning and preparation, word order, breaking up long sentences, organising ideas into paragraphs and sentences, being concise and avoiding redundancy, ambiguity and vagueness

Unit – II **6**

Interpreting research findings, understanding and avoiding plagiarism, paraphrasing sections of a paper/ abstract.

Unit- III **6**

Key skills to frame a title, to draft an abstract, to give an introduction

Unit – IV **6**

Skills required to organise review of literature, methods, results, discussion and conclusions

Unit – V **6**

Usage of appropriate phrases and key terms to make the writing effective - proof-reading to ensure error-free writing.

Text Books:

1. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011
2. Highman N , Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book, 1998.
3. Day R, How to Write and Publish a Scientific Paper, Cambridge University Press, 2006.
4. Goldbort R, Writing for Science, Yale University Press, 2006. (available on Google Books)

REFERENCES

Martin Cutts, Oxford Guide to Plain English, Oxford University Press, Second Edition, 2006

Total: 30 hours

Dr. M. Renuga
BoS – Chairperson,
Science & Humanities
HOD / H&L

ECE-VLSI
III

Sona College of Technology, Salem
(An Autonomous Institution)
Courses of Study for ME III Semester under Regulations 2019
Electronics and Communication Engineering
Branch: M.E. VLSI Design

S. No	Course Code	Course Title		Lecture	Tutorial	Practical	Credit	Total Hours
Theory								
1	**P19VLD506**	**Professional Elective-** Embedded Systems		3	0	0	3	45
2	**P19VLD511**	**Professional Elective-** Analysis and Design of Digital Integrated Circuits		3	0	0	3	45
3	**P19MIT601**	**Open Elective**	Python Programming	3	0	0	3	45
Practical								
4	**P19VLD301**	Project Phase - I		0	0	16	8	240
						Total Credits	**17**	**375**

Approved by

5/7/2023

Chairman, Electronics and Communication Engineering BOS
Dr.R.S.Sabeenian

Member Secretary, Academic Council
Dr.R.Shivakumar

Chairperson, Academic Council & Principal
Dr.S.R.R.Senthil Kumar

Copy to:-
HOD/ECE, Third Semester ME VLSI Students and Staff, COE

M.E-ECE
VLSI
III

P19VLD506 **EMBEDDED SYSTEMS** 3 0 0 3

Course Outcomes

At the end of the course, the students will be able to,

1) Illustrate the basic architecture of embedded system
2) Analyze the ARM and SHARC processors
3) Analyze and describe about the different networks in the embedded system
4) Compute the real time characteristics of embedded system
5) Design the techniques used to describe the embedded system design

CO/PO, PSO Mapping

(3/2/1 indicates strength of correlation) 3-Strong, 2-Medium, 1-Weak

COs	Programme Outcomes (POs) and Programme Specific Outcome (PSOs)													
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	P09	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	3	3	3	3	1	2	1		1	1	2	2
CO2	3	3	3	3	3	3	1	2	1		1	1	2	2
CO3	3	3	3	2	2	3	1	2	1		1	1	2	2
CO4	3	3	3	2	2	3	1	2	1		1	1	2	2
CO5	3	3	3	3	3	3	1	2	1		1	1	2	2

Unit I EMBEDDED ARCHITECTURE **09**

Embedded Computers – Characteristics of Embedded Computing Applications – Challenges in Embedded System Design – Embedded System Design Process – Requirements – Specification and Architectural Design – Designing Hardware and Software Components – System Integration.

Unit II EMBEDDED PROCESSOR AND COMPUTING PLATFORM **09**

ARM Processor – Processor and Memory Organization – Data Operations – Flow of Control – SHARC Processor Memory Organization – Data Operations – Flow of Control – Parallelism with instructions – CPU Bus Configuration – ARM Bus – SHARC Bus – Memory Devices – Input / Output Devices – Design Example: Alarm Clock..

05.07.2023

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Regulations- 2019

Unit III NETWORKS 09

Distributed Embedded Architecture – Hardware and Software Architectures – Networks for Embedded Systems – Multitasking and multi threading - Specifications and data format of I^2C, CAN Bus – SHARC link ports – Ethernet – Myrinet –Design Example: Elevator Controller.

Unit IV REAL-TIME CHARACTERISTICS 09

Clock Driven Approach – Weighted Round Robin Approach – Priority Driven Approach – Dynamic versus Static Systems – Effective Release Times and Deadlines – Optimality of the Earliest Deadline First (EDF) Algorithm – Off-line Versus On-Line Scheduling

Unit V SYSTEM DESIGN TECHNIQUES 09

Design Methodologies – Requirement Analysis – Specification – System Analysis and Architecture Design – Quality Assurance – Design Example: Telephone PBX-Ink Jet Printer – Personal Digital Assistants – Set-Top Boxes.

TOTAL : 45 HOURS

References

1) Wayne Wolf, "*Computers as Components: Principles of Embedded Computing System Design*", Morgan Kaufman Publishers, 2009
2) Jane. W.S. Liu, "*Real-Time systems*", Pearson Education India, 2006
3) Frank Vahid and Tony Givargis, "*Embedded System Design: A Unified Hardware/Software Introduction*", John Wiley & Sons, 2006.
4) Krishna C. M. and Shin K. G., "*Real-Time Systems*", McGraw-Hill Education, 2017.

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P19VLD511 ANALYSIS AND DESIGN OF DIGITAL INTEGRATED CIRCUITS 3 0 0 3

Course Outcomes

At the end of each unit, the students will be able to

1) Explain the digital integrated circuits, devices-bipolar and MOS
2) Analyze the fabrication, layout and simulation and MOS inverter circuits
3) Analyze of the high speed CMOS logic design and dynamic logic design.
4) Discuss about the semiconductor memory design
5) Examine the interconnect design and power grids

CO/PO, PSO Mapping

(3/2/1 indicates strength of correlation) 3-Strong, 2-Medium, 1-Weak

COs	Programme Outcomes (POs) and Programme Specific Outcome (PSOs)													
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	P09	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	3	3	3	3	1	2	1		1	1	2	2
CO2	3	3	3	3	3	3	1	2	1		1	1	2	2
CO3	3	3	3	2	2	3	1	2	1		1	1	2	2
CO4	3	3	3	2	2	3	1	2	1		1	1	2	2
CO5	3	3	3	3	3	3	1	2	1		1	1	2	2

Unit I DEEP SUBMICRON DIGITAL IC DESIGN, TRANSISTORS AND DEVICES MOS AND BIPOLAR **09**

Review of Digital Logic Gate Design-Digital IC Design – Computer Aided Design of Digital Circuits – The MOS Transistor – Bipolar Transistor And Circuits – IC Fabrication Technology – Layout Basics – Modeling The MOS Transistor for Circuit Simulation – SPICE MOS Level1 Device Model – BSIM3 Model-Additional Effects in MOS Transistors – SOI Technology.

Unit II FABRICATION, LAYOUT AND SIMULATION, MOS INVERTER CIRCUITS **09**

Voltage Transfer Characteristics – Noise Margin Definitions – Resistive Load Inverter Design – NMOS Transistors as Load Devices – CMOS Inverter-Pseudo – NMOS Inverters – Sizing Inverters – Tristate Inverters.

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Unit III **HIGH SPEED CMOS LOGIC DESIGN, TRANSFER GATE AND DYNAMIC LOGIC DESIGN** **09**

Switching Time Analysis – Detailed Load Capacitance Calculation – Improving Delay Calculation With Input Slope - Gate Sizing For Optimal Path Delay – Optimizing Path With Logical Effort – Basic Concepts of Transfer Gate – CMOS Transmission Gate Logic – Dynamic D Latches And D Flip-Flops – Domino Logic – Voltage Bootstrapping..

Unit IV **SEMICONDUCTOR MEMORY DESIGN, ADDITIONAL TOPICS IN MEMORY DESIGN** **09**

Introduction MOS Decoders – Static RAM Cell Design – SRAM Column I/O Circuitry – Memory Architecture – Content Addressable Memories – FPGA – Dynamic Read – Write Memories – Read Only Memories – EPROMs And EEPROMs – Flash Memory – FRAMs.

Unit V **INTERCONNECT AND POWER GRID AND CLOCK DESIGN** **09**

Interconnect RC Delays – Buffer Insertion for Very Long Wires – Interconnect Coupling Capacitance – Interconnect Inductance – Antenna Effects – Power Distribution Design – Clocking and Timing Issues – Phase- Locked Loops – Delay-Locked Loops

TOTAL : 45 HOURS

References

1) David A Hodges, Horace G Jackson, Resve A Saleh, "*Analysis and design of Digital Integrated Circuits – in deep submicron technology*", Tata McGraw Hill, Edition 2005.
2) Sung-Mo Kang, Yusuf Leblebici, "*CMOS Digital Integrated Circuits-analysis and design*", Tata McGraw Hill, Third edition, 2003.

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P19MIT601 **PYTHON PROGRAMMING** **3 0 0 3**

PREAMBLE

Python is an easy to learn, powerful programming language. It has efficient high-level data structures. It is a simple but effective approach to object-oriented programming. Python's elegant syntax and dynamic typing, together with its interpreted nature, make it an ideal language for scripting and rapid application development in many areas on most platforms. This programming language has become a preferred development technology in IT industries.

Python can be integrated with many other technologies also. It is rapidly becoming a de-facto language for data analytics and / or machine learning as many packages are added to perform more complex tasks. This course aims to teach everyone the basics of programming using Python.

COURSE OUTCOMES

At the end of the course, the student will be able to

1. Write simple applications
2. Develop programs using loops
3. Create applications using functions
4. Develop application using files
5. Create application using Python and MySQL

CO / PO, PSO Mapping
(3/2/1 indicates strength of correlation) 3-Strong, 2-Medium, 1-Weak

COs	Programme Outcomes (POs) and Programme Specific Outcome (PSOs)													
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	P09	PO10	PO11	PO12	PSO1	PSO2
CO1	3	3	3									3	3	3
CO2	3	3	3									3	3	3
CO3	3	3	3									3	3	3
CO4	3	3	3									3	3	3
CO5	3	3	3									3	3	3

UNIT I INTRODUCTION **9**

The way of programming-What is programming- debugging – formal and natural languages - Python: Features - Installing - Running – The Basics-variables-Operators and Expressions

UNIT II CONTROL FLOW **9**

Control Flow: introduction- if – else – while statement – do while – for loop –break – continue

UNIT III PYTHON FUNCTIONS **9**

Sequences: String - List – Tuple – Dictionary - Functions – Function Parameters, Local and Global Variables, Default Arguments, Keyword Arguments, Return Statements.

UNIT IV PYTHON MODULES, PACKAGES AND FILES **9**

Introduction – Byte files – from import – making own modules – Files and Input/Output: File Objects and Built in functions – Command line Arguments – Packages.

J. Akilandeswari

Dr. J. AKILANDESWARI
PROFESSOR & HEAD
Department of Information Technology
SONA COLLEGE OF TECHNOLOGY
SALEM-636 005

UNIT V PYTHON DATABASE CONNECTIVITY 9

SQL Introduction – simple queries – create - insert – update – delete, MySQL Introduction – connecting python and MySQL database.

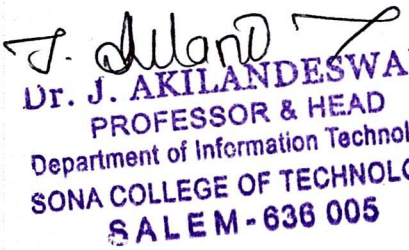
Total: 45 hours

TEXT BOOK

1. Swaroop C N, " A Byte of Python ", ebshelf Inc., 1st Edition, 2013.

REFERENCES

1. Wesley J. Chun, "Core Python Programming", Pearson, 2nd Edition, 2006.
2. Allen B.Downey, "Think Python: How to Think Like a Computer Scientist", O'Reilly Media, 2nd Edition, 2015.



M.E.VLSI
IV

Sona College of Technology, Salem
(An Autonomous Institution)
Courses of Study for ME IV Semester under Regulations 2019
Electronics and Communication Engineering
Branch: M.E. VLSI Design

S. No	Course Code	Course Title	Lecture	Tutorial	Practical	Credit	Total Contact Hours
Practical							
1	P19VLD401	Project Phase -II	0	0	28	14	420
					Total Credits	**14**	

Approved by

22/12/2023

Chairperson, Electronics and Communication Engineering BOS
Dr.R.S.Sabeenian

Member Secretary, Academic Council
Dr.R.Shivakumar 26/12/23

Chairperson, Academic Council & Principal
Dr.S.R.R.Senthil Kumar

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